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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,511	11/26/2001	Kie Y. Ahn	500466.02	1533

7590 07/08/2002

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EXAMINER	
RAMSEY, KENNETH J	
ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 07/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Offic Action Summary	09/994,511	AHN ET AL.	
	Examiner	**Art Unit**	
	Kenneth J. Ramsey	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 & 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Prior Art Rejections

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 52 is rejected under 35 U.S.C. 102(b) as being anticipated by Jones (5,529,524). Jones discloses a process of forming an FED display including a porous dielectric comprising the steps of forming a polycrystalline silicon layer 354, column 28, line 67 through column 29, line 2, on a substrate and a plurality of column electrodes 351. Subsequently Jones et al , at column 29, lines 19-21, forms pores in the polysilicon layer and oxidizes the silicon. Thus claim 52 is clearly anticipated.

3. Claims 52- 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (5,458,518) in view of Jones. Lee, column 3, lines 43-66, teaches a method of forming a porous dielectric layer in a field emitter display comprising anodizing a portion of a silicon substrate to form a porous silicon layer and oxidizing at a temperature of 1,000 °C. Lee differs in that there is no disclosure of depositing a poly-silicon layer prior to anodizing. Jones teaches a similar process of forming a dielectric layer in a field emission display and teaches depositing a poly-silicon layer 354 over the cathode column lines 351 prior to treating the poly-silicon to form a porous dielectric layer. It would have been obvious for one of ordinary skill to include a step of forming column lines in the substrate of Lee prior to forming the dielectric layer, since it is well known to provide addressable field emission sites by such a process. Therefore, to provide a poly-silicon layer in Lee prior to forming the dielectric thereover would have been obvious to one of ordinary skill in the art.

4. Claims 42-46, 49, 50, 56, 59, 60 and 62-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Jones as above applied with respect to claim 52 further in view of Glade et al (5,569,058). Lee differs from claims 42 and 56 in that the field emitters are not formed after the dielectric layer and extraction grid (gate layer) are formed and cavities are etched therein. This process is a well known alternative for forming the emitters as shown by Glade et al. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to form the emitters 21 of Lee subsequent to the step of forming the dielectric layer and extraction grid, by the process of Gnade et al

since it is a well known alternative. As to claims 76-77 and 83-94, Lee taught an oxidizing temperature greater than 1000 °C. As to claims 70 and 75, the columnar nature of anodized porous silicon is well known. As to claims 43 -45, 62-69, 71-74 and 78-82, Gnade et al, column 2, line 60 through column 3, line 30 and column 3, lines 48-54 teach that it was desired to have a high porosity gate insulator in a field emitter display to achieve a low dielectric constant. Further, Gnade et al taught a high porosity silicon dioxide dielectric having a dielectric constant less than 2 (column 5, lines 37-48 and column 8, lines 30-31). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have chosen an anodizing time and power sufficient to achieve a high porosity, low dielectric constant gate insulator in Lee as modified by Jones '524 in view of Gnade et al.

5. Claims 47, 48, 51, 57, 58 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, Jones '524 and Gnade et al as applied to claims 42 and 56 above, and further in view of Jones et al (5,663,608). Lee et al differs from these claims in that a metal doped silicon nonoxide field emitter which is coated with a low work function emissive coating is not taught. However, it was known in the art of field emission displays to form a metal doped silicon monoxide emitter which is coated with a low work function emissive material. See Jones et al '608, column 15, lines 27-30. Further, a doped silicon monoxide emitter is advantageous because it provides a resistive emitter which provides for uniform emission from plural emitters and a low work function coating is advantageous because of a reduced power requirement. Therefore it would

have been obvious to one of ordinary skill in the art at the time of applicant's invention to provide metal doped silicon monoxide field emitters in Lee as modified above in order to obtain uniform field emission with a reduced power requirement. As to claims 48 and 58, Official notice is taken that it was known in the process steps of Borel et al to evaporate the emissive material at an angle perpendicular to the substrate to achieve a high aspect ratio of emitter height to base diameter and it is well known to deposit doped silicon by coevaporation of silicon and a metal..

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aboaf et al teaches the anodization/thermal oxidation process for obtaining a porous silicon dioxide dielectric. Yue et al teaches an anodization/oxidation process to form a porous silicon dioxide layer 16 in a field emission device.

Directions for Responses

Any formal response to this communication should be directed to examiner Kenneth Ramsey, Art Unit 2879, and either faxed to: 703-872-9318; or mailed to: Assistant Commissioner For Patents

Washington, D.C. 20231

Technical inquiries concerning this communication should be directed to Kenneth J. Ramsey, (703) 308-2324 (voice), (703) 746-4832 (fax).

Kenneth J. Ramsey
Primary Examiner
Art Unit 2879